IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Douglas D. Coolbaugh, et al. **Examiner:** Unassigned

Serial No: 10/605,439 **Art Unit:** Unassigned

Filed: 9/30/03 **Docket:** BUR920020094US1 (16895)

For: PRECISION POLYSILICON RESISTOR PROCESS **Dated:** 11/13/03

Commissioner for Patents
United States Patent Office
Alexandria, VA 23313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. Japanese Patent Publication No. JP5275619, dated October 22, 1993;

2. C.H. Lee, IBM Disclosure Bulletin "Polysilicon Resistors Compatible with Bipolar Integrated Circuits ad Method of Manufacture", Vol. 25, No. 5, October 1982; and

3. G.R. Goth, et al., IBM Disclosure Bulletin "Planar Self-Aligned Metal/Sidewall and Polysilicon-Resistor Process", Vol. 25, No. 2, July 1982.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Box 1450, Alexandria, VA 22313-1450 on

Dated: 11/13/03

Maryann Lussi
Maryann Lussi

Applicants are submitting copies of the above-cited references.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,

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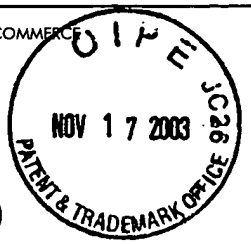
Enclosure PTO 1449
Three (3) references

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE
(REV. 7-80)PATENT AND TRADEMARK OFFICE

LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)



Atty. Docket N .	Serial N .
BUR920020094US1 (16895)	
Applicant Douglas D. Coolbaugh, et al.	
Filing Date	**Group** Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
	AA						
	AB						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
		JP5275619	10/22/1993	JAPAN				

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		C.H. Lee, IBM Disclosure Bulletin "Polysilicon Resistors Compatible with Bipolar Integrated Circuits ad Method of Manufacture", Vol. 25, No. 5, October 1982; and
		G.R. Goth, et al., IBM Disclosure Bulletin "Planar Self-Aligned Metal/Sidewall and Polysilicon-Resistor Process", Vol. 25, No. 2, July 1982.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.